IN THE CLAIMS

Please replace all prior claims in the present application with the following claims, in which claims 3, 12, and 20 are canceled without prejudice or disclaimer, and claims 1, 10, and 18 are currently amended.

1. (Currently Amended) A method for transmitting encoded signals, the method comprising:

receiving one of a plurality of set of bits of a codeword from ~~an~~ a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword;

non-sequentially mapping, according to the structure of the codeword, the one set of bits into a higher order constellation; and

outputting a symbol of the higher order constellation corresponding to the one set of bits based on the mapping.

2. (Original) A method according to claim 1, further comprising:

writing *N* encoded bits to a block interleaver on a column by column basis; and

reading out the encoded bits on a row by row basis, wherein the block interleaver has *N*/3 rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying), *N*/4 rows and 4 columns when the higher order modulation is 16-APSK (Amplitude Phase Shift Keying), and *N*/5 rows and 5 columns when the higher order modulation is 32-APSK.

3. (Canceled)

4. (Original) A method according to claim 3, wherein the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.

5. (Original) A method according to claim 3, wherein the higher order constellation represents a Quadrature Phase Shift Keying (QPSK) modulation scheme, the method further comprising:

determining an i^{th} QPSK symbol based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2..., N/2-1, and N is the coded LDPC block size.

6. (Original) A method according to claim 3, wherein the higher order constellation represents an 8-PSK modulation scheme, the method further comprising:

determining an i^{th} 8-PSK symbol based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

7. (Original) A method according to claim 3, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, the method further comprising:

determining an i^{th} 16-APSK symbol based on the set of $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

8. (Original) A method according to claim 3, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, the method further comprising:

determining an i^{th} 32-APSK symbol based on the set of $(N/5+i)^{th}$, $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.

9. (Original) A computer-readable medium bearing instructions for transmitting encoded signals, said instruction, being arranged, upon execution, to cause one or more processors to perform the method of claim 1.

10. (Currently Amended) A transmitter for generating encoded signals, the transmitter comprising:

~~an~~ a binary Low Density Parity Check (LDPC) encoder configured to transform an input message into a codeword represented by a plurality of set of bits; and

logic configured to map non-sequentially, according to the structure of the codeword, one set of bits into a higher order constellation, wherein a symbol of the higher order constellation corresponding to the one set of bits is output based on the mapping.

11. (Original) A transmitter according to claim 10, wherein the *N* encoded bits are written to a block interleaver column by column and read out row by row, and the block interleaver has *N*/3 rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying), *N*/4 rows and 4 columns when the higher order modulation is 16-APSK (Amplitude Phase Shift Keying), and *N*/5 rows and 5 columns when the higher order modulation is 32-APSK.

12. (Canceled)

13. (Original) A transmitter according to claim 12, wherein the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.

14. (Original) A transmitter according to claim 12, wherein the higher order constellation represents a Quadrature Phase Shift Keying (QPSK) modulation scheme, and the logic is further configured to determine an i^{th} QPSK symbol based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2..., N/2-1, and N is the coded LDPC block size.

15. (Original) A transmitter according to claim 12, wherein the higher order constellation represents an 8-PSK modulation scheme, and the logic is further configured to determine an i^{th} 8-PSK symbol based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

16. (Original) A transmitter according to claim 12, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, and the logic is further configured to determine an i^{th} 16-APSK symbol based on the set of bits $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

17. (Original) A transmitter according to claim 12, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, and the logic is further configured to determine an i^{th} 32-APSK symbol based on the set of bits $(N/5+i)^{th}$, $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.

18. (Currently Amended) A method for processing encoded signals, the method comprising:

demodulating a received Low Density Parity Check (LDPC) encoded signal representing a codeword, wherein the encoded signal being modulated according to a non-sequential mapping, based on the structure of the codeword, of a plurality of bits corresponding to the codeword; and

decoding the codeword associated with the encoded signal.

19. (Original) A method according to claim 18, wherein the N encoded bits are written to a block interleaver column by column and read out row by row, and the block interleaver has $N/3$ rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying), $N/4$ rows and 4 columns when the higher order modulation is 16-APSK (Amplitude Phase Shift Keying), and $N/5$ rows and 5 columns when the higher order modulation is 32-APSK.

20. (Canceled)

21. (Original) A method according to claim 20, wherein the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.

22. (Original) A method according to claim 20, wherein the higher order constellation represents a Quadrature Phase Shift Keying (QPSK) modulation scheme, and an i^{th} QPSK symbol is determined based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein $i=0,1,2\ldots$, $N/2-1$, and N is the coded LDPC block size.

23. (Original) A method according to claim 20, wherein the higher order constellation represents an 8-PSK modulation scheme, and an i^{th} 8-PSK symbol is determined based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein $i=0,1,2,\ldots,N/3-1$, and N is the coded LDPC block size.

24. (Original) A method according to claim 20, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, and an i^{th} 16-APSK symbol is determined based on the set of bits $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein $i=0,1,2,\ldots,N/3-1$, and N is the coded LDPC block size.

25. (Original) A method according to claim 20, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, and an i^{th} 32-APSK symbol is determined based on the set of bits $(N/5+i)^{th}$, $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.

26. (Original) A computer-readable medium bearing instructions processing encoded signals, said instruction, being arranged, upon execution, to cause one or more processors to perform the method of claim 18.